REMARKS

This paper is being provided in response to the Office Action mailed December 10, 2004, for the above-referenced application. In this response, Applicant has cancelled claim 13 without prejudice or disclaimer of the subject matter thereof and amended claims 12 and 18 to clarify that which Applicant considers to be the invention. Applicant respectfully submits that the amendments to the claims are fully supported by the originally-filed specification. Further, as noted below, Applicant submits herewith a verified translation of the Japanese patent application to which the present U.S. application claims priority.

The objection to claim 12 for informalities has been addressed according to the guidelines as set forth in the Office Action. Accordingly, Applicant respectfully requests that this objection be reconsidered and withdrawn.

The rejection of claims 12-17, 19 and 20 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,184,083 to Tsunashima et al. (hereinafter "Tsunashima") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein. Claim 13 is cancelled herein.

Independent claim 12, as amended herein, recites a method of manufacturing a complementary integrated circuit. A semiconductor substrate is prepared. A region for forming an n-channel element and a region for forming a p-channel element are formed on the semiconductor substrate via an element isolation region. A dummy gate electrode is formed in each of said regions for forming n-channel and p-channel elements. N-type diffusion regions are

formed in the region for forming an n-channel element and p-type diffusion regions are formed in the region for forming a p-channel element. The n-type diffusion regions are formed by implanting an n-type impurity into said region for forming an n-channel element by using a first mask, said first mask including: (1) said dummy gate formed in said region for forming an n-channel element and (2) a first resist film covering said region for forming a p-channel element. The p-type diffusion regions are formed by implanting a p-type impurity into said region for forming a p-channel element by using a second mask, said second mask including: (1) said dummy gate formed in said region for forming a p-channel element and (2) a second resist film covering said region for forming an n-channel element. An insulating film is formed over the entire surface of the semiconductor substrate. The dummy gate formed in one of said regions for forming n-channel and p-channel elements is removed to form a first trench in the insulating film. The first trench is filled with a gate electrode material. The dummy gate formed in the other of said regions for forming n-channel and p-channel elements is removed to form a second trench in the insulating film. The second trench is filled with a gate electrode materiál. Claims 14-17, 19 and 20 depend directly or indirectly on independent claim 12.

The Tsunashima reference discloses a semiconductor device and method of manufacturer. First and second films are formed at a plurality of regions on a substrate at which gate electrodes are to be formed. The first and second films are removed and a first insulator film and a first gate electrode are formed at one of the plurality of regions from which the first and second films have been removed. (See col. 3, lines 36-53 and Figs. 5A-D and 7A-F of Tsunashima.)

Applicant's independent claim 12, as amended, recites at least the features that a method for manufacturing a complementary integrated circuit includes forming n-type and p-type diffusion regions, wherein the n-type and p-type regions are separately formed by implantation of impurities using first and second masks, the masks including respective dummy gates and first and second resist films formed over specific regions used to form the n-channel and p-channel elements, as is claimed by Applicant. Applicant has found that a method of manufacturing a complementary integrated circuit as claimed allows for gate materials of nMOSFETs and pMOSFETS to be separately deposited from the implantation of impurities used to form the diffusion regions in a desired manner. Consequently, because the implantation is performed using the dummy gates and resin films as masks, the gate materials are restrained from becoming depleted, and the manufacturing procedure facilities the use of a plurality of gate materials in which gates are buried in trenches resulting in an enhanced manufacturing technique that is easy to perform and capable of achieving miniaturization. (See, for example, page 31, lines 19-30 of the present application.)

Applicant respectfully submits that Tsunashima does not teach or fairly suggest at least the above-noted features as claimed by Applicant. Specifically, the Office Action suggests that the use of dummy gates and masks in the configuration as claimed by Applicant to produce diffusion regions is inherent. However, Applicant respectfully traverses this conclusion and points out that Applicant discloses a specific procedure whereby diffusion regions are produced in an easy and efficient manner while gate materials are configured as desired in trenches and depletion of the gate materials is restrained as a result of the method. Applicant submits that the method as claimed by Applicant is not inherent to the manufacture of an integrated circuit in that

other procedures can be used to prepare deposition regions but which do not offer the above-noted benefits of the present claimed invention. Accordingly, Applicant respectfully submits that Tsunashima does not disclose the above-noted features as claimed by Applicant. In view of the above, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 21, 23 and 24 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,489,191 to Shao et al. (hereinafter "Shao") is hereby traversed and reconsideration is respectfully requested.

The Shao reference discloses a method for forming self-aligned channel implants using a gate polyreverse mask.

Submitted herewith is a verified translation of Japanese Patent Application No. 11-052323 (the Japanese Priority Application), to which the present application claims priority. The Japanese Priority Application was filed on March 1, 1999 and supports claims 12-27 of the present U.S. application. See, for example, page 12, line 1 to page 13, line 29 of the verified translation. Accordingly, Applicant respectfully submits that the verified translation of the Japanese Priority Application entitles the above-referenced application to the priority date of March 1, 1999.

Applicant respectfully submits that the date of the Japanese Priority Application, March 1, 1999, is prior to the earliest effective filing date of the Shao reference, December 17, 1999.

Accordingly, Applicant respectfully requests that Shao be withdrawn and that this rejection of Applicant's claims in view of Shao also be withdrawn.

The rejection of claims 18 and 25 under 35 U.S.C. 103(a) as being unpatentable over Tsunashima and Shao in view of U.S. Patent No. 6,130,123 to Liang et al. (hereinafter "Liang") is hereby traversed and reconsideration is respectfully requested. Applicant has rewritten claim 18 into independent form.

The Liang reference discloses a method for making a complementary metal gate electrode including a transistor having a metal gate electrode overlying a gate dielectric on an area of a semiconductor substrate. The Office Action cites Liang as disclosing that first and second gate electrodes of a CMOS device may be formed of zirconium and nickel respectively.

As noted above, Applicant respectfully submits that the date of the Japanese Priority Application, March 1, 1999, is prior to the earliest effective filing date of the Shao reference, December 17, 1999. Accordingly, Applicant respectfully requests that Shao be withdrawn and that this rejection of Applicant's claims in view of Shao also be withdrawn.

The rejection of claim 22 under 35 U.S.C. 103(a) as being unpatentable over Shao in view of U.S. Patent No. 6,291,282 to Wilk et al. (hereinafter "Wilk") is hereby traversed and reconsideration is respectfully requested.

The Wilk reference discloses method of forming dual metal gate structures of CMOS devices. The Office Action cites Wilk as disclosing a gate insulator formed in a trench and a gate material formed over the gate insulator.

As noted above, Applicant respectfully submits that the date of the Japanese Priority Application, March 1, 1999, is prior to the earliest effective filing date of the Shao reference, December 17, 1999. Accordingly, Applicant respectfully requests that Shao be withdrawn and that this rejection of Applicant's claims in view of Shao also be withdrawn.

The rejection of claims 26 and 27 under 35 U.S.C. 103(a) as being unpatentable over Shao in view of Tsunashima is hereby traversed and reconsideration is respectfully requested.

As noted above, Applicant respectfully submits that the date of the Japanese Priority Application, March 1, 1999, is prior to the earliest effective filing date of the Shao reference, December 17, 1999. Accordingly, Applicant respectfully requests that Shao be withdrawn and that this rejection of Applicant's claims in view of Shao also be withdrawn.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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